IN THE CLAIMS

1-4. (canceled)

5. (currently amended) A method of generating target instructions from a plurality of first instructions, the target instructions executable on a target processor, comprising:

analyzing the plurality of first instructions en masse by an information processing system to break down the functional operations encoded by the first instructions to produce information representing ~~an information~~ a flow of information ~~in accordance with the first instructions~~ to be handled efficiently by the target processor to achieve results on the target processor equivalent to the results intended to be achieved by the first instructions;

generating the target instructions by an information processing system based on the information representing the information flow, in preference over particular operations specified by individual ones of the plurality of first instructions.

6. (previously presented) A method as claimed in claim 5, wherein the first instructions are not executable on the target processor.

7. (previously presented) A method for executing target instructions generated according to a method as claimed in claim 5, wherein the information representing the information flow is produced and the target instructions are generated at run-time, after accessing the plurality of first instructions from a predetermined memory, the method further comprising executing the target instructions without requiring the target instructions to be first stored to the predetermined memory.

8. (previously presented) A method of generating target instructions as claimed in claim 5, wherein individual ones of the target instructions are generated without regard to particular operations specified by the individual ones of the plurality of first instructions.

9. (currently amended) A method as claimed in claim 5, wherein the plurality of first instructions are according to a first machine language, the plurality of first instructions being ~~and~~ of a type executable by a first processor but not executable by the target processor, and the target instructions are according to a second machine language, the target instructions being ~~and~~ of a type executable by the target processor.

10. (previously presented) A method as claimed in claim 5, wherein the target instructions are generated in a manner to reduce a number of machine cycles required to execute the target instructions.

11. (previously presented) A method as claimed in claim 10, wherein the number of machine cycles is reduced in relation to the number of machine cycles that would be required to execute instructions according to a literal translation of the plurality of first instructions into the second machine language.

12. (previously presented) A method as claimed in claim 9, wherein the target instructions specify a target number of transfers between a register of the target processor and a memory associated with the target processor, the target number being reduced in relation to a number of transfers specified by the plurality of first instructions between a register of the

first processor and a memory associated with the first processor.

13. (previously presented) A method as claimed in claim 12, wherein the target number of transfers is further reduced in relation to a number of transfers resulting from a literal translation of the plurality of first instructions into the second machine language.

14. (previously presented) A method as claimed in claim 12, wherein the target instructions are generated so as to minimize the target number of transfers.

15. (previously presented) A method as claimed in claim 12, wherein the number of transfers is further reduced by reducing a number of transfers of a particular operand between the register of the target processor and the memory associated with the target processor, the operand required for execution of each of a plurality of the target instructions.

16. (previously presented) A method as claimed in claim 5, wherein at least one of the target instructions is generated to specify a second physical operation that is different from, but equivalent to a first physical operation specified by one or more instructions of the plurality of first instructions.

17. (previously presented) A method as claimed in claim 16, wherein the at least one target instruction is equivalent in context to the first physical operation.

18. (previously presented) A method as claimed in claim 9, wherein the first processor has a first number of registers and the target processor has a second number of registers which is

4

less than the first number, wherein the target instructions are generated so as to reduce a number of transfers between a register of the target processor and a memory associated with the target processor.

19.   (currently amended) A method according to claim 5, further comprising determining a purpose to be achieved by the plurality of first instructions en masse, and wherein the step of generating the target instructions includes eliminating operations specified by the plurality of first instructions which are unnecessary to achieve the determined purpose.

20.   (previously presented) A method according to claim 5, further comprising eliminating operations specified by the plurality of first instructions which are unnecessary to support the information flow.

21.   (previously presented) A method as claimed in claim 5, wherein the step of generating the target instructions includes translating first operations specified by the plurality of first instructions to target operations different from the first operations to reduce the number of machine cycles required to execute the target instructions.

22.   (currently amended) A method as claimed in claim 5, further comprising determining a purpose to be achieved by the plurality of first instructions en masse, the purpose being determined by determining a sequence of operations specified by the plurality of first instructions, and removing ones of the specified operations from the sequence which are unnecessary to support the determined purpose, wherein the target instructions are generated after the unnecessary operations are removed from the sequence.

5

23. (currently amended) A method as claimed in claim 5, wherein a target instruction of the target instructions is generated by selecting a target an instruction from a plurality of target instructions specifying respective equivalent operations performable by the target processor, the target instruction being selected in a manner to reduce a number of machine cycles required to execute the selected target instruction relative to another one of the target instructions which specifies the equivalent operation.

24. (currently amended) A machine-readable medium having information recorded thereon for performing a method of generating target instructions from a plurality of first instructions, the target instructions executable on a target processor, the method comprising:

analyzing the plurality of first instructions en masse by an information processing system to break down the functional operations encoded by the first instructions to produce information representing a flow of an information flow to be handled efficiently by the target processor to achieve results on the target processor equivalent to the results intended to be achieved by an information flow in accordance with the first instructions;

generating the target instructions by an information processing system based on the information representing the information flow, in preference over particular operations specified by individual ones of the plurality of first instructions.

25. (previously presented) A machine-readable medium as claimed in claim 24, wherein the information representing the information flow is produced and the target instructions are

6

generated at run-time, after accessing the plurality of first instructions from a predetermined memory, the method further comprising executing the target instructions without requiring the target instructions to be first stored to the predetermined memory.

26. (currently amended) A machine-readable medium as claimed in claim 24, wherein the plurality of first instructions are according to a first machine language, the plurality of first instructions being and of a type executable by a first processor but not executable by the target processor, and the target instructions are according to a second machine language, the target instructions being and of a type executable by the target processor.

27. (previously presented) A machine-readable medium as claimed in claim 26, wherein the target instructions specify a target number of transfers between a register of the target processor and a memory associated with the target processor, the target number being reduced in relation to a number of transfers specified by the plurality of first instructions between a register of the first processor and a memory associated with the first processor.

28. (previously presented) A machine-readable medium as claimed in claim 27, wherein the number of transfers is further reduced in relation to a number of transfers resulting from a literal translation of the plurality of first instructions into the second machine language.

29. (previously presented) A machine-readable medium as claimed in claim 27, wherein the number of transfers is further reduced by reducing a number of transfers of a particular

7

operand between the register and the memory associated with the target processor, the operand required for execution of each of a plurality of the target instructions.

30. (currently amended) A machine-readable medium according to claim 24, wherein the method further comprises determining a purpose to be achieved by the plurality of first instructions en masse, and the step of generating the target instructions includes eliminating operations specified by the plurality of first instructions which are unnecessary to achieve the determined purpose.

31. (previously presented) A machine-readable medium as claimed in claim 24, wherein the step of generating the target instructions includes translating first operations specified by the plurality of first instructions to target operations different from the first operations, to reduce the number of machine cycles required to execute the target instructions.

32. (currently amended) An information processing system operable to generate a plurality of target instructions from a plurality of first instructions, the target instructions executable on a target processor, the system being operable to analyze the plurality of first instructions en masse to break down the functional operations encoded by the first instructions to produce information representing an a flow of information to be handled efficiently by the target processor to achieve results on the target processor equivalent to the results intended to be achieved by the first instructions, and to generate the target instructions based on the information representing the information flow, in preference over particular operations specified by individual ones of the plurality of first instructions.

33. (currently amended) A system as claimed in claim 32, wherein the plurality of first instructions are according to a first machine language, the plurality of first instructions being and of a type executable by a first processor but not executable by the target processor, and the system is operable to generate the target instructions according to a second machine language, the target instructions being and of a type executable by the target processor.

34. (previously presented) A system as claimed in claim 33, wherein the system is operable to generate the target instructions such that, upon execution of the target instructions, a number of transfers between a register of the target processor and a memory associated with the target processor is reduced in relation to the number of transfers specified by the plurality of first instructions between a register of the first processor and a memory associated with the first processor.

35. (previously presented) A system as claimed in claim 34, wherein the system is operable to further reduce the number of transfers between the target processor and the memory associated therewith in relation to a number of transfers resulting from a literal translation of the plurality of first instructions into the second machine language.

36. (previously presented) A system as claimed in claim 34, wherein the system is further operable in relation to transfers specified by the plurality of first instructions, to reduce a number of transfers of a particular operand between the register of the target processor and the memory associated with

the target processor, the operand required for execution of each of a plurality of the target instructions.

37. (previously presented) A system according to claim 32, wherein the system is operable to generate the target instructions so as to eliminate operations specified by the plurality of first instructions which are unnecessary to achieve the determined purpose.

38. (previously presented) A system as claimed in claim 32, wherein the system is operable to generate the target instructions so as to translate first operations specified by the plurality of first instructions to target operations different from the first operations, to reduce a number of machine cycles required to execute the target instructions.

39. (currently amended) A system operable to generate target instructions from a plurality of first instructions, the target instructions executable by a target processor, the system comprising:

a first stage operable to analyze the plurality of first instructions en masse to break down first functional operations encoded by the plurality of first instructions to produce information representing a first flow of information specified by the plurality of first instructions;

a second stage responsive to the first flow of information operable to specify a second flow of information for performing second operations to achieve results equivalent to the results intended to be achieved by the first operations, in preference over particular first operations specified by individual ones of the plurality of first instructions, the second flow of information adapted for more efficient execution on the target processor than the first flow of information; and

a third stage operable to generate target instructions from the second flow of information, wherein the third stage is operable to generate the target instructions through operation including selecting operation codes of instructions from among a plurality of operation codes specifying different but equivalent physical operations.

40. (new) A method of generating target instructions from a plurality of first instructions, the target instructions executable on a target processor, comprising:

analyzing the plurality of first instructions en masse by an information processing system to break down the functional operations encoded by the first instructions to produce information representing a flow of information to be handled efficiently by the target processor to achieve results on the target processor equivalent to the results intended to be achieved by the first instructions; and

generating the target instructions by an information processing system based on the information representing the information flow, in preference over particular operations specified by individual ones of the plurality of first instructions,

wherein said step of analyzing includes omitting an operation encoded by a given one of said plurality of first instructions from said information flow when said operation is overridden by another operation encoded by a second one of said plurality of first instructions.

41. (new) A method of generating target instructions from a plurality of first instructions, the plurality of first instructions being according to a first machine language and being executable by a first processor but not executable by a target processor, and the target instructions being according

11

to a target machine language and being executable by a target processor, the method comprising:

analyzing the plurality of first instructions according to the first machine language en masse by an information processing system to break down the functional operations encoded by the first instructions to produce information representing a flow of information to be handled efficiently by the target processor to achieve results on the target processor equivalent to the results intended to be achieved by the first instructions; and

generating the target instructions according to the target machine language by an information processing system based on the information representing the information flow, in preference over particular operations specified by individual ones of the plurality of first instructions.

42. (new) A method of generating target instructions from a plurality of first instructions, the target instructions executable on a target processor, comprising:

analyzing the plurality of first instructions en masse by an information processing system to break down the functional operations encoded by the first instructions to produce information representing a flow of information to be handled by the target processor to achieve results on the target processor equivalent to the results intended to be achieved by the first instructions, the first instructions specifying a first number of transfers between a register of the first processor and a memory associated with the first processor; and

generating the target instructions by an information processing system based on the information representing the information flow in preference over particular operations specified by individual ones of the plurality of first instructions, the target instructions specifying a target

12

number of transfers between a register of the target processor and a memory associated with the target processor, the target number being reduced in relation to the first number.

43. (new) A method of generating target instructions from a plurality of first instructions executable on a first processor using a plurality of first registers of the first processor, the target instructions being executable on a target processor using a plurality of target registers of the target processor, comprising:

analyzing the plurality of first instructions en masse by an information processing system to break down the functional operations encoded by the first instructions to produce information representing a flow of information to be handled efficiently by the target processor to achieve results on the target processor equivalent to the results intended to be achieved by the first instructions; and

generating the target instructions by an information processing system based on the information representing the information flow, in preference over particular operations specified by individual ones of the plurality of first instructions,

wherein the step of generating the target instructions includes mapping a usage of the target registers in accordance with the target instructions to a usage of the first registers in accordance with the first instructions based on the information representing the information flow, and the mapping varies with time in accordance with the equivalent results sought to be achieved by executing the target instructions on the target processor.